Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. § 102, has acquired an accepted definition, *i.e.*, "the disclosure in the prior art of a thing substantially identical with the claimed invention." *In re Schaumann*, 572 F.2d 312, 197 USPQ 5 (CCPA 1978). To satisfy the burden of establishing a basis for denying patentability under 35 U.S.C. §102, therefore, each and every element of the claims under rejection must be shown by the Office Action to be disclosed in Ker.

Independent claim 1 recites, *inter alia*, the following:

> a first input terminal receiving a first positive voltage externally in an inspection of said semiconductor device and a normal operation of said semiconductor device;
> an internal circuit connected to said first input terminal and performing a prescribed operation; and
> a first protection circuit protecting said internal circuit from static electricity generated at said first input terminal . . . .

Independent claim 4 recites similar requirements.

In the present invention, the claimed protection circuit is not internal to a circuit but is disconnected after test. The protection circuit is also provided to a plurality of power supply terminals and connected to a common reference potential line. Typically, the terminal can receive only a positive voltage (for example, 10v), only a negative voltage (for example, -5v), or both positive and negative voltages. The protection circuit includes diodes provided in a number of stages and of polarity determined by the value of voltage applied and its polarity.

The Office Action has read the first input terminal, recited in claim 1on the VDD terminal 805 of Ker (Fig. 8). Ker, however, describes the protection circuit as protecting against static electricity generated at the input pad 801, not at the first input terminal as required by claim 1. Ker discloses a protection circuit internal to a circuit. The protection circuit includes a diode connected

between a VDD power supply and GND. A surge applied to an input pad is discharged to the VDD power supply and GND.

Furthermore, as the protection circuit is internal to the circuit, the protection circuit will never be disconnected. There is no disclosure in Ker that terminal 805 receives an external positive voltage in an inspection of the semiconductor device and in normal operation as required by claim 1. Moreover, Ker's input pad 801is not readable on the claimed first input terminal and its particular relationship with the protection circuit as recited in the latter paragraphs of claim 1. In addition, there is no nothing in the Ker disclosure to indicate that terminal 801 receives an external voltage that is applied for inspection of the semiconductor device. In summary, it is submitted that Ker lacks disclosure of the above-identified claimed features and, therefore, does not meet the requirements for anticipation of claim 1 under 35 U. S. C. § 102. Claim 4, which differs from claim 1 in reciting an input terminal that receives an external negative voltage, otherwise is distinguishable from Ker for the same reasons as discussed above.

Claim 2, which is dependent from claim 1, is submitted to be patentably distinct from Ker for at least the same reasons as discussed above with respect to its parent claim. Similar deficiencies appear with respect to claim 2, not only with respect to the requirements of claim 1, but as to the further requirements relating to the second input terminal recited. The Office Action reads the second input terminal as the VSS (GND) supply rail 806. The Office Action has not identified what element in Ker is believed to correspond to the claimed line of reference potential. As lines 805 and 806 are already spoken for, it appears that the line connected to input pad 801 has been intended to meet this claimed element. Such a reading is in contradiction both with the claims, when appropriately interpreted in light of the application disclosure, and the disclosure of Ker. As disclosed in the present application, a line of reference potential is ground line 40 (Fig. 3). A person

of ordinary skill in the art, in contemplation of Ker, would have understood a line of reference potential in the Ker arrangement to have been either the positive supply VDD or the negative ground supply VSS. It would have made no sense to an artisan to identify a line connected to an input pad, whose input is unknown and apparently neither VDD nor VSS, as a line of reference potential.

Claim 5 has been rejected under 35 U. S. C. § 103(a) as being unpatentable over U.S. patent 5,953,191 (Narita) in view of Ker. Legal precedent is well developed on the subject of obviousness. In the application of a rejection under 35 U.S.C. §103, it is incumbent upon the examiner to factually support a conclusion of obviousness. *In re Mayne,* 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997*); In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). As stated in *Graham v. John Deere Co.* 383 U.S. 1, 13, 148 USPQ 459, 465 (1966), obviousness under 35 U.S.C. §103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art. The examiner must provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

In order to establish the requisite motivation, "clear and particular" factual findings must be made as to a specific understanding or specific technological principle which would have realistically compelled one having ordinary skill in the art to modify a particular reference to arrive at the claimed invention based upon facts-- not generalizations. *Ruiz v. A.B. Chance Co.*, 234 F.3d

654, 57 UPSQ2d 1161 (Fed. Cir. 2000); *Ecolochem Inc. v. Southern California Edison, Co.* 227 F.3d 361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Kotzab*, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). In addition, the Examiner is required to explain **why** one having ordinary skill in the art would have been realistically motivated to modify a particular reference in a particular manner to arrive at a particular claimed invention; *Ecolochem Inc. v. Southern California Edison, Co. supra;. In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). Such motivation, of course, regardless of its source, must be based upon "clear and particular" showings in the prior art -- not in the application disclosure; *In re Dembiczak, supra.; Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985).

Claim 5 is reproduced below.

> 5. A semiconductor device comprising:
> an input terminal receiving externally a voltage of at most a first positive voltage and at least a first negative voltage in an inspection of said semiconductor device and a normal operation of said semiconductor device;
> an internal circuit connected to said input terminal and performing a prescribed operation; and
> a protection circuit protecting said internal circuit from static electricity generated at said input terminal,
> said protection circuit including
> a plurality of first diode elements connected in series between said input terminal and a line of a reference potential and conducting in response to a voltage of said input terminal exceeding a second positive voltage higher than said first positive voltage, and
> a plurality of second diode elements connected in series between the line of said reference potential and said input terminal and conducting in response to the voltage of said input terminal going lower than a second negative voltage lower than said first negative voltage.

The claimed protection circuit discharges an applied surge to the common reference potential line. Accordingly, a single terminal is provided for discharge. Typically (and in test) the

terminal can receive only a positive voltage (for example 10v), only a negative voltage (for example -5v) or both positive and negative voltages. The protection circuit includes diodes provided in a number of stages and having a polarity determined by the value of voltage applied and its polarity. The protection circuit employs the same device as the internal circuit and does not require an additional process. It can be formed of a p or n channel TFT alone, and is applicable not only to CMOS process but also single channel (p or n channel) process.

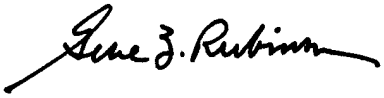
Narita is stated in the Office Action to differ from the requirements of claim 5 with respect to the diode element recitation for the protection circuit. Ker has been relied upon, at paragraph 2 of the Office Action, for concluding that it would have been obvious to use a plurality of diodes in Narita. It is submitted that there is no description in Narita of inspection of a semiconductor device as required by the claim. In addition, in Narita, if a surge pulse of a voltage positive with respect to VSS terminal 4 is applied to input terminal 3, the surge is discharged to VSS terminal 4. The common discharge line is a line for discharge, and the discharge is done via each of a plurality of terminals. For each terminal, a single diode and a single voltage clamp element are provided. Furthermore, the protection circuit is a device different from the internal circuit, and an extra process is accordingly required. Modification of the Narita arrangement to contain the diode configuration of Ker, it is submitted, is not a mere variation but an undertaking that would not have been suggested to the artisan, let alone a compelling one. A modification such as proposed in the Office Action involves a substantial reconstruction of the Narita arrangement for which there is no teaching from the combined disclosures of these references.

Accordingly, withdrawal of the rejections and allowance of the application are respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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